CLOCK SIGNAL GENERATING DEVICE

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Abstract of **JP63044215**

PURPOSE:To prevent the number of read only memory devices from being increased, by using the memory device in a time division mode.

CONSTITUTION:A clock signal generating device is constituted of a read only memory device 30 in which plural different clock signal patterns are stored along a bit wire, an address signal generation circuit 20 which generates an address signal from the signal of a master clock signal circuit 1, and generates the addresses of plural number of clock signal patterns time-divisionally, flip-flop circuits 40 and 60 which separate and output a parallel clock pattern respectively. In the address signal generation circuit 20, the most significant bit of the address signal is changed to values '0' and '1' according to a master clock signal. And the addresses of both patterns are designated by time division by using the above change, and it is possible to output the clock signal pattern from the read only memory device 30 as a serial time division signal.